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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,054	08/26/2003	Matthew Russell	03-0154	2925

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,054	RUSSELL ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Initially, and with respect to claims 1and 6, note that a limitation in a claim with respect to the manner in which a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device teaches all structural limitations in the claims and the functional limitations are found to be inherent in the prior art device. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See *Hewlett-Packard Co. v. Bausch & Lomb Inc.* and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a device claim, and not the patentability of its functions (909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). As stated in Best, Where the claimed and prior art products are identical or substantially identical in structure or composition, a *prima*

facie case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). Note that the applicant has burden of proof once the examiner establishes a sound basis for believing that the products of the applicant and the prior art are the same. See *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated or, in the alternative, under 35 U.S.C. 103(a) as obvious over Nogami et al. (US 6,060,383).

4. Regarding claim 1, Nogami (e.g. figs. 10 and 15) shows a power bus layout design comprising: a first electrically conductive layer 45 including at least a first power bus and a second power bus, a second electrically conductive layer 43 including at least a first power bus and a second power bus, an electrically insulating layer disposed between the first electrically conductive layer and the second electrically conductive layer, a plurality of vias 75 (see fig. 5; i.e. 70) through the electrically insulating layer 54 conductively connecting the first electrically conductive layer and the second electrically conductive layer and arranged such that the first power bus and the second power bus of the first electrically conductive layer are electrically connected.

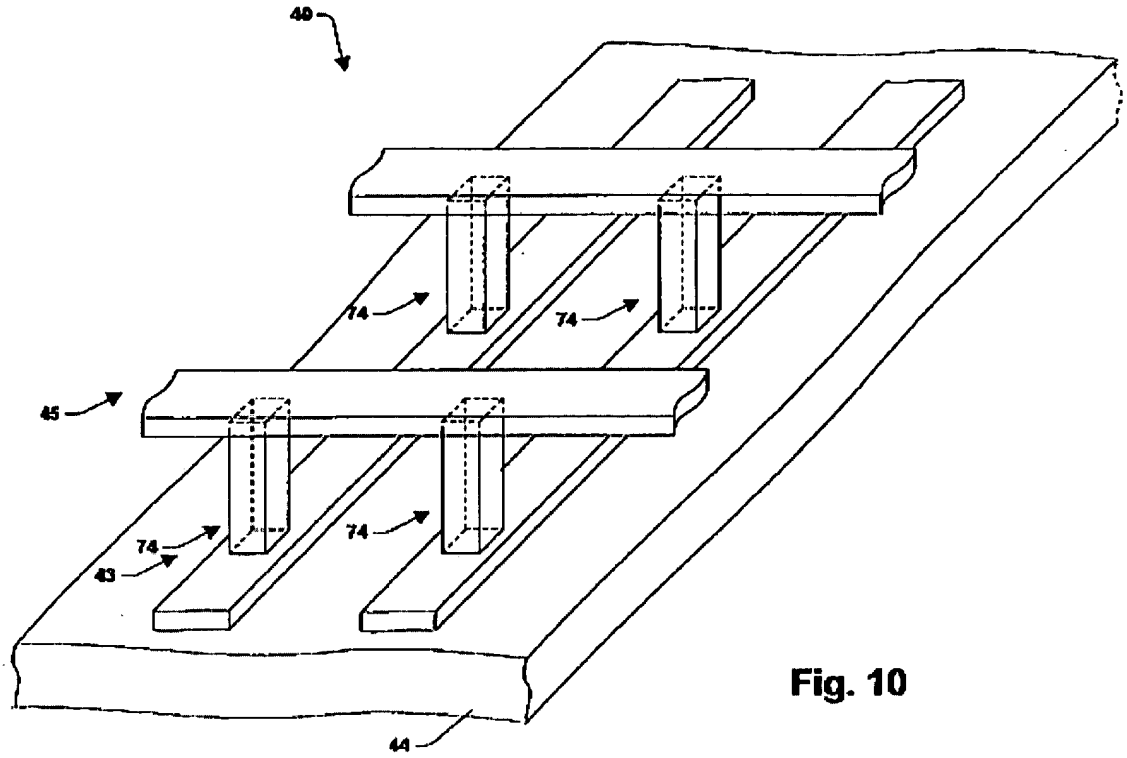

Fig. 10

In reference to the language in claim 1referring to the function of the bus layout, it is noted that Nogami shows all structural aspects of the semiconductor device according to the instant invention (emphasis added, see paragraph 4) and *that providing a power supply current on the first power bus and the second power bus of the first layer and on the first power bus and the second power bus of the second layer to reduce bottlenecking of the power supply current*, is an intended use and/or function that does not affect the structure of the final device. As taught by Nogami the first and second electrically conductive layer are supplied with a voltage (col. 1/lls. 19-28). Furthermore, it is expected that the prior art will produce the same result under the same claimed scenario (i.e. *to reduce bottlenecking of the power supply current*) since

every claimed structural limitation were disclosed. As to the grounds of rejection of claim 1 under section 103, see MPEP § 2112, which discusses the handling of functional language in the claims and recommends the alternative (§ 102/ § 103) grounds of rejection.

5. Regarding claim 2, Nogami shows that the plurality of vias connecting the first electrically conductive layer and the second electrically conductive layer are arranged such that the first power bus and the second power bus of the second electrically conductive layer are electrically connected

6. Regarding claim 3, Nogami shows that the first and second power bus of the first electrically conductive layer overlap the second power bus of the second electrically conductive layer.

7. Regarding claim 4, Nogami shows that the first and second power buses of the first electrically conductive layer overlap the first and second power buses of the second electrically conductive layer across the entire input/output width.

8. Regarding claim 5, Nogami shows that the plurality of vias connecting the first electrically conductive layer and the second electrically conductive layer are arranged such that the first power bus and the second power bus of the second electrically conductive layer are electrically connected; and wherein the first and second power bus of the first electrically conductive layer overlaps the first and second power bus of the electrically conductive layer; across the entire input/output width.

9. Regarding claim 6, Nogami (e.g. figs. 10 and 15) a power bus layout design comprising: a first electrically conductive layer 45 including a plurality of power buses

not conductively connected to each other on the first electrically conductive layer; a second electrically conductive layer 43 including a plurality of power buses not conductively connected to each other on the second electrically conductive layer; an electrically insulating layer 45 disposed between the first electrically conductive layer and the second electrically conductive layer; and wherein at least one power bus on the first electrically conductive layer is conductively connected to at least one power bus on the second electrically conductive layer through the electrically insulating layer. In reference to the language in claim 6 referring to the function of the bus layout, it is noted that Nogami shows all structural aspects of the semiconductor device according to the instant invention (emphasis added, see paragraph 4) and *that providing a power supply current on the first power bus and the second power bus of the first layer and on the first power bus and the second power bus of the second layer to reduce bottlenecking of the power supply current*, is an intended use and/or function that does not affect the structure of the final device. As taught by Nogami the first and second electrically conductive layer are supplied with a voltage (col. 1/lls. 19-28). Furthermore, it is expected that the prior art will produce the same result under the same claimed scenario (i.e. *to reduce bottlenecking of the power supply current*) since every claimed structural limitation were disclosed. As to the grounds of rejection of claim 1 under section 103, see MPEP § 2112, which discusses the handling of functional language in the claims and recommends the alternative (§ 102/ § 103) grounds of rejection.

10. Regarding claim 7, Nogami shows at least one power bus on the first electrically conductive layer overlaps with at least one power bus on the second electrically conductive layer.

11. Regarding claim 8, Nogami shows a plurality of vias 75 (see fig. 5; i.e. 70) through the electrically insulating layer, the vias conductively connect at least one power bus on the first electrically conductive layer to at least one power bus on the second electrically conductive layer.

Response to Arguments

12. Applicant's arguments filed 06/21/2005 have been fully considered but they are not persuasive.

13. In response to applicant's argument that Nagomi is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Nagomi is directed to a multilevel interconnection structure for semiconductor devices (see col. 1/lls. 10-19) which is the same field of endeavor of the application (see applicant's disclosure, page 2/lls. 1-5). The fact that instant invention and the prior art are directed to solve different problems, which are commonly present in the multilayered interconnection structures of semiconductor devices, does not imply that both inventions belong to different field of endeavor. Additionally, Applicant's argument that the prior art is not in the same field of endeavor since its disclosure is primary directed to fabrication

method, was not found persuasive because disclosed method produce a multilayered interconnection structure including every claimed structural limitation. It is respectfully noted that both inventions belong to the same field of endeavor (i.e. multilayered interconnection structure for semiconductor devices).

14. In response to applicant's argument that prior art does not teach that the disclosed structure reduce bottlenecking of the power supply current, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner
Art Unit 2826
08/15/2005